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Method of manufacturing a semiconductor device and semiconductor device obtained with such a method

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Method of manufacturing a semiconductor device and semiconductor device obtained with such a method

The invention relates to a method of manufacturing a semiconductor device in which a semiconductor body of silicon is provided at a surface thereof with a semiconductor region of the first conductivity in which region a second semiconductor region of a second, opposite to the first, conductivity type is formed forming a pn-junction with the first semiconductor region by introducing dopant atoms of the second conductivity type into the semiconductor body and wherein before the introduction of said dopant atoms an amorphous region is formed in the semiconductor body by means of an amorphizing implantation and wherein after the amorphizing implantation temporary dopant atoms are implanted in the semiconductor body and wherein after introduction of the dopant atoms of the second conductivity type the semiconductor body is annealed by a heat treatment thereof.

Such a method is very suitable for making devices with very shallow, steep and low-ohmic pn-junctions and in particular for making MOSFET (= Metal Oxide Semiconductor Field Effect Transistor) devices. In the future CMOS (=Complementary MOS) technology such a pn-junction is among others required for the formation of source and drain extensions. This is in particular not easy for future so-called sub 65 nm technologies.

A method as mentioned in the opening paragraph is known from US patent application US 2003/0109119 A1 that has been published on June 12, 2003. Therein such a method is described in which a MOSFET is made using for forming the source and drain extensions the formation of a pn-junction in the manner described above. First an amorphizing implantation is done; next an implantation of temporary dopant atoms in the form of Fluor atoms is performed. The dopant atoms in the form of Boron atoms are introduced in the semiconductor body by means of out diffusion from a layer of solid material deposited on the surface of the semiconductor body and containing a sufficient concentration of the dopant atoms like boron. Finally, the semiconductor body is annealed using a short heat treatment in the temperature range of about 950 degrees Celsius to about 1100 degrees Celsius.

A drawback of such a method is that the pn-junctions obtained are still not always shallow, steep and low ohmic enough for future requirements.

It is therefore an object of the present invention to avoid the above drawbacks and to provide a method, which does provide very shallow, steep and low-ohmic pn-junctions for in particular the formation of source and drain extensions of MOSFETs.

To achieve this, a method of the type described in the opening paragraph is characterized in that the dopant atoms of the second conductivity type are introduced into the semiconductor body by means of ion implantation and the semiconductor body is annealed by a heat treatment at a temperature in the range of about 500 to about 800 degrees Celsius. The invention is firstly based on the recognition that ion implantation, which is a very well industrial applicable process, is suitable for forming very shallow, steep and low-ohmic pn-junctions provided that the thermal budget of the process is limited. A further insight is that the annealing process of the known method still contributes significantly to said budget due to its relatively high temperature. Diffusion of the dopant atoms like boron cannot sufficiently be prevented during such a step. The invention is further based on the surprising recognition that annealing at intermediate temperatures, e.g. in the range from 800 to 950 degrees Celsius, is not suitable because at these temperature a deactivation occurs of the Boron atoms which is accompanied with an increase of the (sheet) resistance of e.g. a source or drain extension which thus is not optimal. Below 500 degrees Celsius the time needed becomes too large or the annealing even does not occurs at all. Finally the invention is based on the recognition that a low temperature is on the one hand suitable for completely annealing the semiconductor body and on the other hand prevents or in any case strongly limits diffusion of the dopant atoms because the time needed for such a low temperature SPE (= Solid Phase Epitaxy) process is still relatively low. The presence of e.g. a fluor profile between the profile of the dopant atoms, not only reduces the diffusion of the dopant atoms but since it separates the so called end of range damage of the amorphizing implantation from the dopant atoms it prevents or in case reduces the deactivation of the dopant atoms which is present at the upper border of the temperature range in a method according to the invention.

Thus, with a method according to the invention a pn-junction is obtainable which is steep and shallow and with a very high doping concentration on one of its sides, i.e. with a low resistance channel. It is to be noted that in a method of the present invention [illegible]

ion implantation for the introduction of the Boron atoms into the semiconductor body. A single anneal has been applied in this document, also at a high temperature ranging from 900 to 1075 degrees Celsius.

In a preferred embodiment the semiconductor body is annealed by a heat treatment at a temperature in the range of 550 to about 750 degrees Celsius. In this way the deactivation of dopant atoms is nearly completely avoided.

Preferably the implantation of the temporary dopant atom is performed before the implantation of the second conductivity type dopant atoms and between these implantations the semiconductor body is annealed by a further heat treatment in the same temperature range as the heat treatment. In this way the influence of the annealing process on the diffusion of dopant atoms can further be limited. In the case that only one annealing step is used at the end of the process the order of the implantations of the temporary dopants and the dopant atoms can be chosen the same although a reverse order is feasible in such a case.

In a further preferred embodiment wherein the semiconductor device is formed as a field effect transistor, in which method the semiconductor body of silicon is provided at the surface thereof with a source region and a drain region of the second conductivity type which both are provided with extensions and with a channel region of the first conductivity type between the source region and the drain region and with a gate region separated from the surface of the semiconductor body by a gate dielectric above the channel region, the first semiconductor region is formed as a part of the channel region and the source and drain extensions are formed by the second semiconductor region. In this way a MOSFET device is obtainable with excellent properties in a future, sub 65 nm, CMOS process. Preferably for the first conductivity type the n-conductivity type is chosen, for the dopant atoms of the second conductivity type Boron atoms are chosen and for the temporary dopant atoms Fluor atoms are chosen. In this way a PMOSFET is obtained. In addition NMOSFETs can be made in the same process and possibly in a similar manner. Other atoms might be used for the temporary dopant atoms, the choice of which might depend on the kind of transistor to be formed.

Preferably, for the amorphizing implantation of inert ions, ions are chosen from a group comprising Ge, Si, Ar or Xe.

Suitable times for the annealing heat treatments are to be found between 1 second and 10 minutes. If only one final heat treatment is used a suitable time at 550 degrees Celsius is about 10 minutes, at 650 degrees Celsius about 1 minute, at 700 degrees Celsius about 20 seconds, and at 750 degrees Celsius about 1 second. If a heat treatment is applied between the temporary and second conductivity type dopant implantations, a suitable time

lies in the range of 20 seconds to 10 minutes. The final heat treatment times are lower in this case, e.g. n the range from 1 minute to 5 seconds in the temperature range from 550 degrees Celsius to 650 degrees Celsius.

The invention also comprises a semiconductor device obtained with a method according to the invention. Preferably such a device comprises a field effect transistor of which the source and drain extensions are made as described above.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter, to be read in conjunction with the drawing, in which

Fig. 1 is sectional view of a semiconductor device obtained with a method according to the invention,

Figs. 2 through 6 are sectional views of the semiconductor device of fig. 1 at various stages in the manufacture of the device by means of a method in accordance with the invention, and

Fig. 7 shows the normalized sheet resistance change of two test samples as a function of the annealing temperature.

The figures are diagrammatic and not drawn to scale, the dimensions in the thickness direction being particularly exaggerated for greater clarity. Corresponding parts are generally given the same reference numerals and the same hatching in the various figures.

Figure 1 is sectional view of a semiconductor device obtained with a method according to the invention. The device 10, which is in this case a PMOST, comprises a semiconductor body 1 that is made of n-type silicon, here formed by an n-type silicon substrate 11. The device 10 contains in practice near its borders isolation regions such as a so-called trench or LOCOS (= Local Oxidation of Silicon) isolation, which however is not shown in the drawing. In practice the device 10 will contain many transistors both of the NMOS and PMOS type. At the surface of the semiconductor body are present a, in this case p-type, source region 2 and drain region 3 provided with – also p-type- extensions 2A,3A that are more shallow and bordering a, in this case n-type, channel region 4 above which a [illegible] is present, separated from the channel region by a gate dielectric 5. In this case

also of silicondioxide, border the gate region 5. On top of the source, drain and gate regions (2,3,5) a metal silicide (8A,8B,8C) is present functioning as connection region.

Figures 2 through 5 are sectional views of the semiconductor device of figure 1 at various stages in the manufacture of the device by means of a method in accordance with the invention. The starting point for the manufacture of the device 10 is (see figure 2) an n-type silicon substrate 11 - or a p-type substrate provided with a so-called n well, which may form the channel region 4 of a PMOST - which here also forms the semiconductor body 1. In the body 1, isolation regions – not shown in the drawing – are formed. Subsequently on the surface of the silicon body 1 a gate dielectric 6 of a silicon oxide is formed, in this case by means a thermal oxidation. Next a polycrystalline silicon layer 5, is deposited on the gate dielectric layer 6 by means of CVD in a usual manner. Its thickness is in this example 100 nm. A mask – not shown in the drawing - is deposited on the structure at the area of the gate 5 to be formed, e.g. comprising a resist and formed by means of photolithography. Outside the mask the layer 5,6 are removed by means of etching and in this way the gate stack, comprising gate 5 and gate dielectric 6, is formed.

Subsequently spacers 20, e.g. of silicondioxide, are formed at both sides of the gate stack by depositing a uniform layer of said material on the device 10 and thereof and by anisotropic etching thereof such that it is again removed in the planar regions of the device. Now a deeper p+ type, in this case of boron ions, implantation I_1 is done in order to form source and drain 2,3. The semiconductor body is then annealed at a temperature of > 1000 °C in order to activate the source and drain implantations.

The spacers 20 than (see figure 3) are removed before making the extensions 2A,3A. This is done in this example by a series of three ion implantations $I_{2,3,4}$. A first implantation I_2 comprises amorphizing of a part of the semiconductor body 1, of which the relevant part in the drawing also is marked I_2, and is done by implanting germanium ions into the semiconductor body 1. In this example at an implantation energy in the range of 10 to 30 keV and with a dose of about 10^{15} at./cm^2. Then a second implantation I_3 is done to form the region I_3 that comprises the temporary dopant atoms, in this case Fluor atoms. This implantation is done at implantation energy in the range of 3 to 10 keV while the implantation dose is also about 10^{15} at./cm^2. Subsequently the semiconductor body 1 is exposed to a first annealing treatment at a temperature of about 600 degrees Celsius during a few minutes.

Next (see figure 4) the semiconductor body 1 is exposed to a third ion implantation I_4 in which the dopant atoms, here Boron atoms, are introduced into the

semiconductor body 1. This is done with an implantation energy between 0,5 and 3 keV and with a dose in the range of about $5x10^{14}$ at./cm^2 to about $5x10^{15}$ at./cm^2. Thus, the position of the fluor implantation is about between the boron profile and the range of the amorphizing implantation. Next the amorphous silicon of the implantations is further recovered in a second annealing process between a temperature of 550 and 750 degrees Celsius. In this case also at a temperature of 600 degrees Celsius and here during 20 seconds.

In this way (see figure 5) a very abrupt and narrow profile of the Boron atoms in the source and drain extensions 2A,3A is obtained while these regions have a very high Boron concentration and thus a very low resistance. Subsequently new spacers 40 are formed in a similar way as described above. This is followed (see figure 6) by the deposition of a metal layer 8, e.g. of titanium, by which after moderate heating silicide regions acting as connection regions are formed. Unreacted parts of the metal layer 8 can be removed by etching after which the structure shown in figure 1 results.

Finally (see figure 8) the manufacturing of the n-MOSFET is further completed by deposition of a pre-metal dielectric, e.g. of silicondioxide, followed by patterning thereof, deposition of a contact metal layer, e.g. of aluminum, again followed by patterning by which contact regions are formed. These steps are not shown in the drawing.

Figure 7 shows the normalized sheet resistance change of two test samples as a function of the annealing temperature. The relative sheet resistance change $\Delta\rho/\rho$, which is normalized with respect to the sheet resistance ρ at 700 degrees Celsius, is shown as a function of temperature T for two samples. Curve 70 corresponds with a test layer formed by the above implantations I_2 and I_4, i.e. the amorphizing and the dopant implantations whereas curve 71 corresponds with a test layer formed by the above mentioned implantations I_2, I_3 and I_4, i.e. the amorphizing, temporary dopant and dopant implantations. Both curves 70,71 show that for an annealing temperature above about 750 degrees an increase of the sheet resistance occurs with a maximum of about 55 % and of about 20 % respectively. At temperatures below 750 degrees, the sheet resistance is not detrimentally influenced in both cases. The difference between the two curves 70,71 shows that the presence of the temporary atoms, in this case fluor atom, has an important beneficial on the increase of the sheet resistance at higher temperatures. Thus, in a method according to the invention a moderate exceeding of the thermal budget envisaged has not much detrimental effect on the quality of a boron doped layer thanks to the presence of the temporary dopant atoms, i.e. the Fluor atoms.

It will be obvious that the invention is not limited to the examples described herein, and that within the scope of the invention many variations and modifications are possible to those skilled in the art.

CLAIMS:

1. Method of manufacturing a semiconductor device (10) in which a semiconductor body (1) of silicon is provided at a surface thereof with a semiconductor region (4) of the first conductivity in which region a second semiconductor region (2A,3A) of a second, opposite to the first, conductivity type is formed forming a pn-junction with the first semiconductor region (4) by introducing dopant atoms of the second conductivity type into the semiconductor body (1) and wherein before the introduction of said dopant atoms an amorphous region is formed in the semiconductor body (1) by means of an amorphizing implantation of inert atoms and wherein after the amorphizing implantation temporary dopant atoms are implanted in the semiconductor body (1) and wherein after introduction of the dopant atoms of the second conductivity type the semiconductor body is annealed by a heat treatment thereof, characterized in that dopant atoms of the second conductivity type are introduced into the semiconductor body (1) by means of ion implantation and the semiconductor body is annealed by a heat treatment at a temperature in the range of about 500 to about 800 degrees Celsius.

2. Method according to claim 1, characterized in that the semiconductor body (1) is annealed by a heat treatment at a temperature in the range of 550 to about 750 degrees Celsius.

3. Method according to claim 1 or 2, characterized in that between the implantation of the temporary dopant atom is performed before the implantation of the second conductivity type dopant atoms and between these implantations the semiconductor body (1) is annealed by a further heat treatment in the same temperature range as the heat treatment.

4. Method according to claim 1, 2 or 3, wherein the semiconductor device is formed as a field effect transistor, in which method the semiconductor body (1) of silicon is provided at the surface thereof with a source region and a drain region (2,3) of the second conductivity type which both are provided with extensions (2A,3A) and with a channel

region (4) of the first conductivity type between the source region and the drain region (2,3) and with a gate region (5) separated from the surface of the semiconductor body (1) by a gate dielectric (6) above the channel region (4), characterized in that first semiconductor region (4) is formed as a part of the channel region (4) and the source and drain extensions (2A,3A) are formed as a part of the second semiconductor region (2A,3A).

5. Method as claimed in anyone of the preceding claims, characterized in that for the first conductivity type the n-conductivity type is chosen, for the dopant atoms of the second conductivity type Boron atoms are chosen and for the temporary dopant atoms Fluor atoms are chosen.

6. Method according to claim 3 or 4, characterized in that for the amorphizing implantation of inert ions, ions are chosen from a group comprising Ge, Si, Ar or Xe.

7. Method as claimed in anyone of the preceding claims, characterized in that for the annealing heat treatments a time is chosen between 1 second and 10 minutes.

8. A semiconductor device (10) obtained with a method as claimed in anyone of the preceding claims.

9. A semiconductor device (10) as claimed in claim 8, characterized in that the device comprises a field effect transistor.

ABSTRACT:

The invention relates to a method of manufacturing a semiconductor device (10) in which a semiconductor body (1) of silicon is provided at a surface thereof with a semiconductor region (4) of the first conductivity in which region a second semiconductor region (2A,3A) of a second, opposite to the first, conductivity type is formed forming a pn-junction with the first semiconductor region (4) by introducing dopant atoms of the second conductivity type into the semiconductor body (1) and wherein before the introduction of said dopant atoms an amorphous region is formed in the semiconductor body (1) by means of an amorphizing implantation of inert atoms and wherein after the amorphizing implantation temporary dopant atoms are implanted in the semiconductor body (1) and wherein after introduction of the dopant atoms of the second conductivity type the semiconductor body is annealed by a heat treatment thereof.

According to the invention the dopant atoms of the second conductivity type are introduced into the semiconductor body (1) by means of ion implantation and the semiconductor body is annealed by a heat treatment at a temperature in the range of about 500 to about 800, preferably from 550 to 750, degrees Celsius. In this way pn-junctions are formed which are very suitable for forming source and drain extensions (2A,3A) of a MOSFET that are very shallow, thermally stable and steep and low ohmic.

Fig. 1

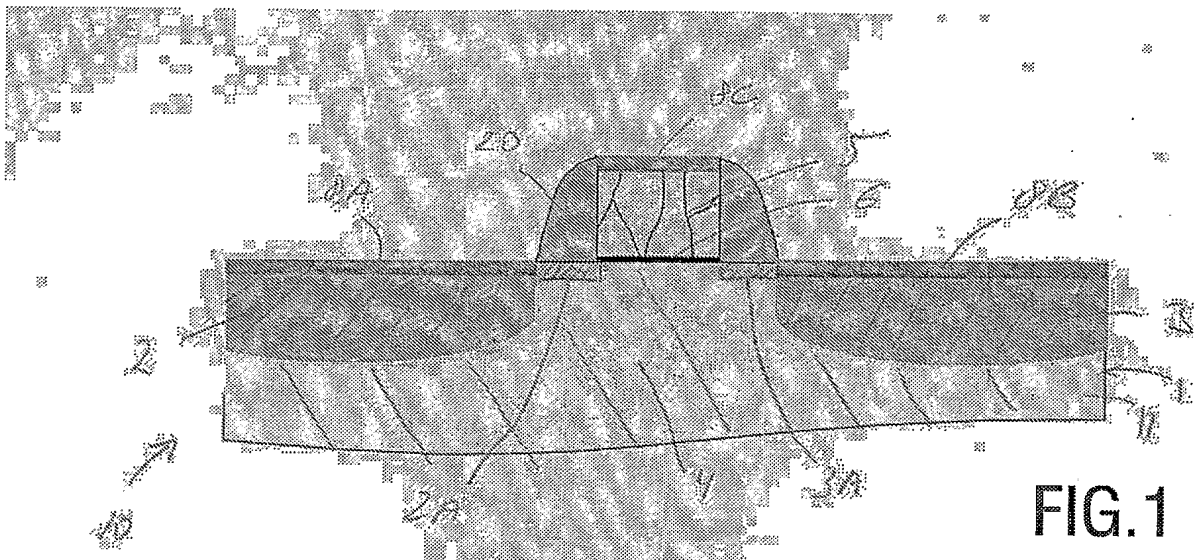

FIG.1

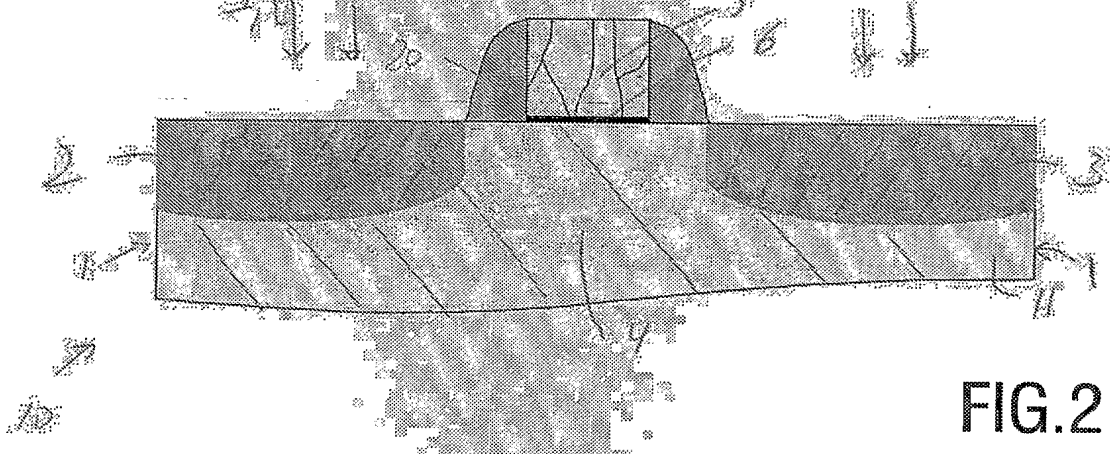

FIG.2

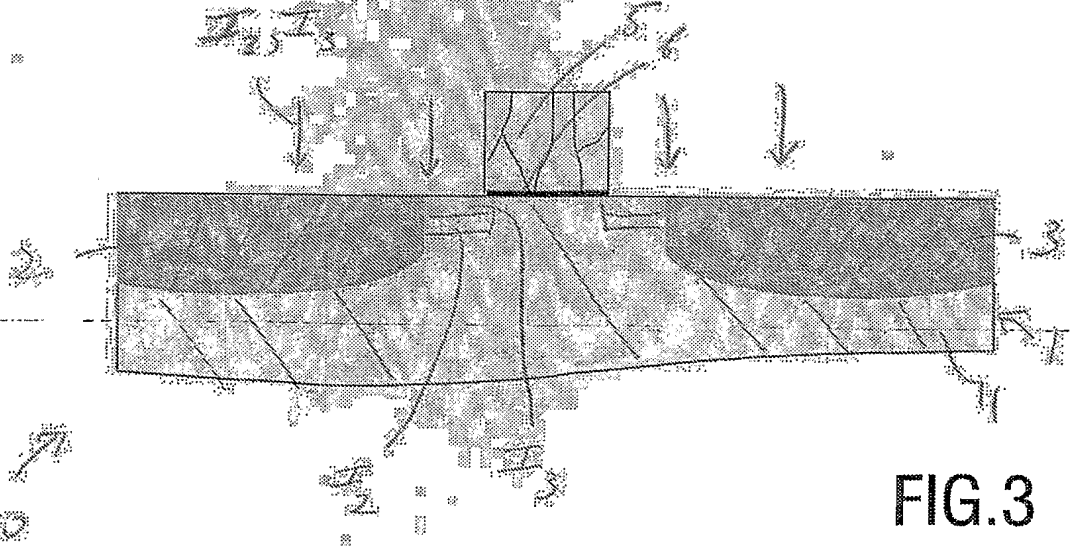

FIG.3

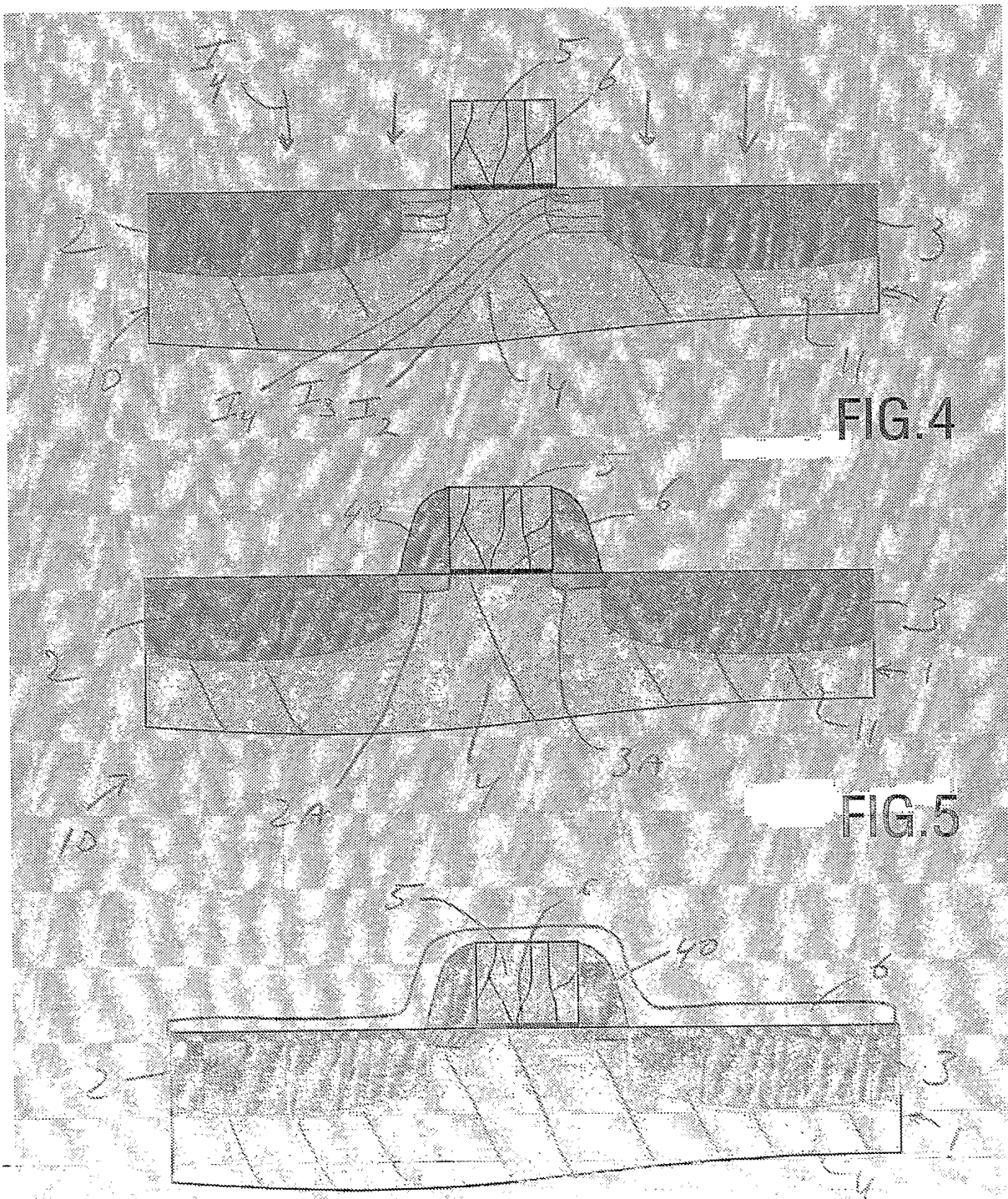

FIG.4

FIG.5

FIG.6

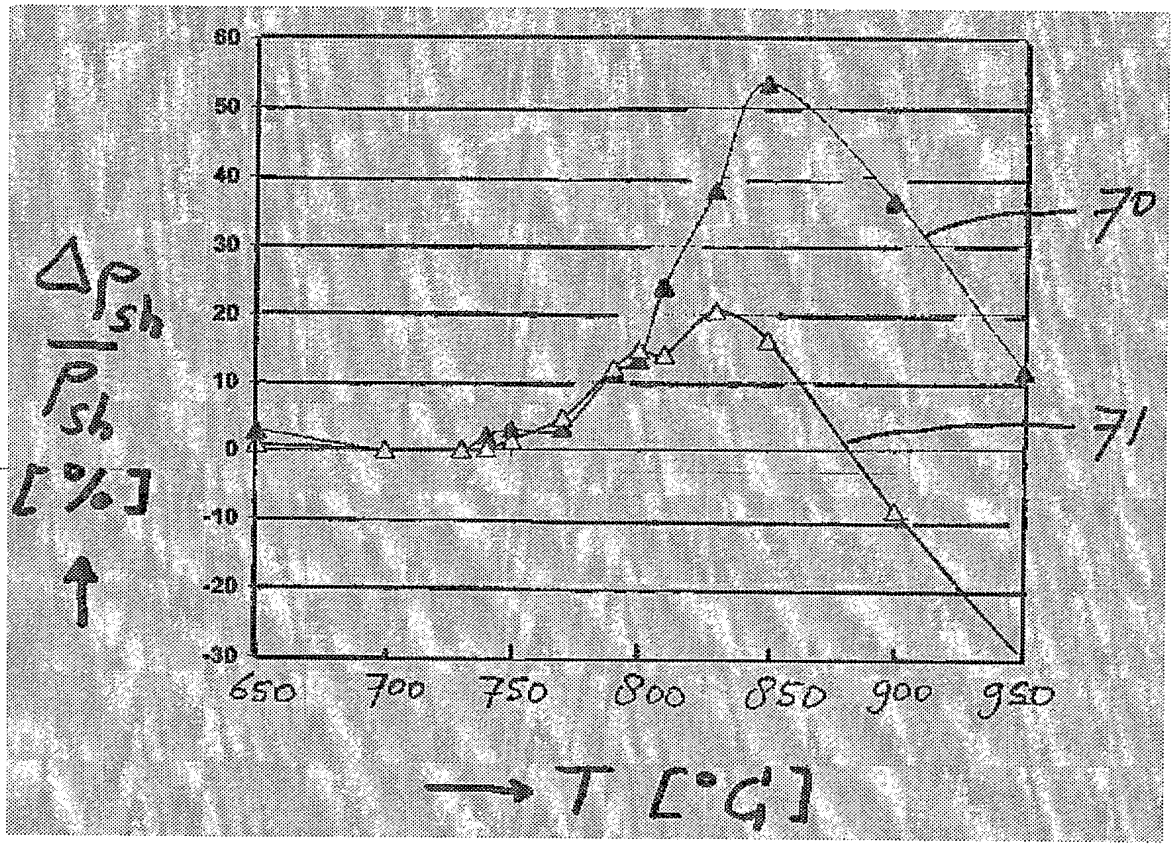
60
50
40
30
20
10
0
-10
-20
-30
650
700
750
800
850
900
950
70
71
$\frac{\Delta\rho_{sh}}{\rho_{sh}}$ [%]
T [°C]

FIG.7

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